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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,451	03/07/2002	Chi Chang	SUND 295	9022

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EXAMINER	
BRINEY III, WALTER F	

ART UNIT	PAPER NUMBER
2646	

DATE MAILED: 03/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,451	CHANG ET AL.	
	Examiner	Art Unit	
	Walter F. Briney III	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18 and 19* is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10 January 2006 has been entered.

Claim Rejections - 35 USC § 112

The previous rejections of claims 4 and 5 under 35 U.S.C. § 112, second paragraph, have been obviated by the applicant's current amendment. As such, the rejections are hereby withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 1-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain (US Patent 6,275,088) in view of Sedra et al. (Microelectronic Circuits, Fourth Edition, 1997, chapter 13, pages 1049-1052).**

Claims 1-11, 14 and 17 were shown to be anticipated by Jain in the Final Office Action filed 10 August 2005. The claims are rejected for the reasons presented in the previous action and for the reasons herein. It is noted that claims 1 and 17 have been amended to recite "an inputted reference voltage," however this limitation doesn't distinguish the applicant's invention from the prior art. Specifically, although Jain fails to disclose "an inputted reference voltage," the difference is overcome by an obvious modification.

It is noted that Jain is directed toward the transmission of digital pulses using CMOS technology. See column 1, lines 17-20, and figure 5, which depicts a plurality of CMOS structures (e.g. 42 and 44). As correctly noted by the applicant, the buffer 36 includes two inverters 50 and 51, neither of which are shown to include an "inputted reference voltage." Primarily, it is noted that Jain fails to specify the structure of the inverters 50 and 51. This inherently leads to one of ordinary skill in the art designing or choosing the use of a known inverter, such as the CMOS inverter illustrated in figure 13.4(a) of Sedra. It is noted that such an inverter's switching threshold is defined in part by the supply voltage V_{DD}. See page 1051, formula (13.8). In this way, V_{DD} corresponds to an "inputted reference voltage."

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the inverters 50 and 51 using CMOS technology inverters as taught by Sedra simply because Jain fails to disclose how to and because the other circuit elements disclosed by Jain are CMOS based. It is noted that using one type of

logic family eliminates the need for interconnects. Therefore, Jain in view of Sedra makes obvious all limitations of the claims.

Claims 12, 13 and 15 were shown to be unpatentable over Jain in the Final Office Action filed 10 August 2005. The claims are rejected for the reasons presented in the previous action and for the reasons herein. With respect to claim 12, it is noted that a 1V CMOS process could have easily been used in the manner set forth in the previous rejection regarding a 3.3 or 1.5V process. Therefore, Jain in view of Sedra makes obvious all limitations of the claims.

2. **Claims 1 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (figure 2) in view of Jain.**

Claims 1 and 16 were shown to be unpatentable over the applicant's admitted prior art (figure 2) in view of Jain in the Final Office Action filed 10 August 2005. The claims are rejected for the reasons presented in the previous action and for the reasons herein. It is noted that the applicant's admitted prior art (figure 2) depicts a comparator that receives an "inputted reference voltage" V_{ref}. Therefore, the applicant's admitted prior art in view of Jain makes obvious all limitations of the claims.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

3. **Claims 18 and 19 are allowed.**

Claim 18 is limited to "an apparatus of ring-back constriction." Claim 18 recites essentially the same limitations as claim 1, with the exception of the "inputted reference voltage." In addition, claim 18 recites that "the level of the transmission line is pulled up" when "the transistor is turned on." This is in complete contrast to the disclosure of Jain, where the transistor 34 turns on and pulls down the transmission line 16. There is no suggestion in the prior art to modify Jain to meet the claim limitation, and thus, claim 18 is allowable over the cited prior art.

Claim 19 is limited to "the apparatus according to claim 18," and thus, is allowable over the cited prior art for at least the same reasons.

Response to Arguments

Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F. Briney III whose telephone number is 571-272-7513. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFB

SINH TRAN
SUPERVISORY PATENT EXAMINER